CLAIMS

What is claimed is:

1	1. A circuit, comprising:
2	a high side switch coupled between an input and a load; and
3	a control circuit coupled to the high side switch, the control circuit adapted
4	to control the high side switch as a function of a voltage across the high side
5	switch.
1	2. The circuit of claim 1 wherein the control circuit is adapted to turn
2	the high side switch on for an on time period when the control circuit senses the
3	voltage across the high side switch crosses below a first threshold while the high
4	side switch is off.
1	3. The circuit of claim 2 wherein the on time period is substantially
2	fixed.
1	4. The circuit of claim 1 wherein the control circuit is adapted to turn
2	off the high side switch before an end of an on time period if the control circuit
3	senses that the voltage drop across the high side switch crosses above a second
4	threshold.

2	off the high s	ide switch for a minimum off time period before the control circuit
3	turns the high	n side switch on again.
1	6.	The circuit of claim 2 wherein the control circuit is adapted to
2	delay the high	n side switch from being turned on for a delay time after the voltage
3	across the high side switch crosses below the first threshold while the high side	
4	switch is off.	
1	7.	The circuit of claim 1 wherein the load comprises a transformer.
1	8.	The circuit of claim 7 wherein the transformer includes a winding,
2	wherein the c	ontrol circuit is coupled to the winding of the transformer.
1	9.	The circuit of claim 1 wherein the high side switch is included in
2	an integrated	circuit.
1	10.	The circuit of claim 9 wherein the integrated circuit comprises the
2	control circui	t.
1	11.	The circuit of claim 1 wherein the circuit is included in a power
2	conversion cir	rcuit.

The circuit of claim 4 wherein the control circuit is adapted to turn

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1	12.	The circuit of claim 1 wherein the high side switch is a metal oxide
2	semiconducto	or field effect transistor (MOSFET).
1	13.	The circuit of claim 1 wherein the control circuit is adapted to turn
2	the high side	switch on for an on time period when the control circuit senses a
3	change in a slope of the voltage across the high side switch over time while the	
4	high side switch is off.	
1	14.	The circuit of claim 13 wherein the on time period is substantially
2	fixed.	
1	15.	The circuit of claim 14 wherein the change in the slope of the
2	voltage acros	s the high side switch over time represents a change in a polarity of
3	the slope of the voltage across the high side switch over time.	
1	16.	The circuit of claim 13 wherein the control circuit is adapted to
2	turn off the h	igh side switch before an end of an on time period if the control
3	circuit senses	s that the voltage drop across the high side switch crosses above a
4	second thresh	nold.

- 1 17. The circuit of claim 1 wherein the control circuit is adapted to keep
- 2 the high side off switch for a minimum off time period following a turn off of the
- 3 high side switch.
- 1 18. The circuit of claim 13 wherein the control circuit is adapted to
- 2 delay the high side switch from being turned on for a delay time after the change
- 3 in the slope of the voltage across the high side switch over time while the high
- 4 side switch is off.
- 1 19. The circuit of claim 1 wherein the input comprises a positive input
- 2 terminal and a negative input terminal, wherein the high side switch is coupled
- 3 between the positive input terminal and the load, the circuit further comprising a
- 4 low side switch coupled between the negative input terminal and the load.
- 1 20. The circuit of claim 19 wherein the low side switch is coupled to a
- 2 second control circuit wherein the second control circuit is adapted to control the
- 3 low side switch as a function of a voltage across the low side switch.
- 1 21. The circuit of claim 20 wherein the low side switch is turned on
- 2 after a delay time for a low side on time period when the voltage across the low
- 3 side switch crosses below a low side threshold while the low side switch is off.

1	23.	The circuit of claim 21 further comprising a feedback circuit
2	coupled between	een the load and the second control circuit to provide a feedback
3	control loop,	wherein the second control circuit is adapted to vary the delay time
4	to regulate po	wer delivered to the load.
1	24.	The circuit of claim 19 wherein the high side switch is turned on
2	for a high sid	e on time period when a voltage across the high side switch crosses
3	below a high	side threshold.
1	25.	The circuit in claim 24 wherein the low side switch is turned on
2	after a delay	time for a low side on time period when a voltage across the low side
3	switch crosses below a low side threshold.	
1	26.	The circuit of claim 25 wherein the high side on time period and
2	the low side	on time period are substantially fixed.
1	27.	The circuit of claim 25 wherein the high side on time period and
2	low side on	time periods are substantially equal.

The circuit of claim 21 wherein the delay time is substantially zero.

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The circuit of claim 25 wherein the high side on time period is 1 28. adjusted to maintain a voltage across the load during the high side on time period 2 substantially equal to the voltage across the load during the low side on time 3 period. 4 The circuit of claim 25 wherein the delay time is substantially zero. 29. 1 The circuit of claim 19 wherein the high side switch is turned on 30. 1 for a high side on time period when a slope of a voltage across the high side 2 switch changes while the high side switch is off. 3 The circuit of claim 30 wherein the low side switch is turned on 31. 1 after a delay time for a low side on time period when a slope of a voltage across 2 the low side switch changes while the low side switch is off. 3 The circuit of claim 31 wherein the high side on time period and 32. 1 the low side on time period are substantially fixed. 2 The circuit of claim 31 wherein the change in the slope of the 33. 1 voltage across the high side and low side switches is a change in a polarity of the 2 slope across the high side and low side switches.

The circuit of claim 31 wherein the high side on time period and 1 34. low side on time periods are substantially equal. 2 The circuit of claim 31 wherein the high side on time period is 35. 1 adjusted to maintain a voltage across the load during the high side on time period 2 substantially equal to the voltage across the load during the low side on time 3 period. 4 The circuit of claim 35 wherein the voltage across the load during 36. 1 the high side on time period is sensed after a delay from the start of the high side 2 on time period. 3 The circuit of claim 35 wherein the voltage across the load during 37. 1 the low side on time period is sensed after a delay from the start of the low side on 2 time period. 3 The circuit of claim 31 wherein the delay time is substantially zero. 1 38. The circuit of claim 31 further comprising a feedback circuit 39. 1 coupled between the load and the second control circuit to provide a feedback 2 control loop, wherein the second control circuit is adapted to vary the delay time 3 to regulate power delivered to the load. 4

2	low side integ	rated circuit.
1 2 3	41. further comprepriod.	The circuit of claim 40 wherein the low side integrated circuit ises the second control circuit to generate the low side on time
1 2	42.	The circuit of claim 40 wherein the low side integrated circuit also sense circuit to sense a turn off of the high side switch.
1 2	43. of the high si	The circuit of claim 42 wherein the sense circuit senses the turn officide switch by monitoring the voltage across the low side switch.
1 2	44. a high side i	The circuit of claim 30 wherein the high side switch is included in ntegrated circuit.
1 2	45.	The circuit of claim 44 wherein the high side integrated circuit prises the control circuit to generate the high side on time period.
1 2	46.	The circuit of claim 45 wherein the high side integrated circuit also a sense circuit to sense a turn off of the high side switch.

The circuit of claim 31 wherein the low side switch is included in a

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1	47. The circuit of claim 46 wherein the sense circuit senses the turn off	
2	of the low side switch by monitoring the voltage across the high side switch.	
1	48. A half bridge circuit, comprising:	
2	a low side switch;	
3	a high side switch coupled to the low side switch;	
4	a low side capacitor coupled to the low side switch;	
5	a high side capacitor coupled to the low side capacitor and the high side	
6	switch; and	
7	a load connected between a junction between the low side switch and high	
8	side switch and a junction between the low side capacitor and the high side	
9	capacitor, wherein the high side switch is adapted to be turned on for a high side	
10	on time period as a function of a voltage across the high side switch in response	
11	the low side switch turning off.	
1	49. The half bridge circuit of claim 48 wherein the low side switch is	
2	adapted to be turned on for a low side on time period following a delay time as a	
3	function of a voltage across the low side switch in response to the high side switch	
4	turning off.	

The circuit of 49 wherein the high side on time period and the low 1 50. side on time period are substantially fixed. 2 The circuit of claim 48 wherein the high side switch is adapted to 51. 1 be turned on for the high side on time period as a function of a slope of the 2 voltage across the high side switch over time. 3 The circuit of claim 48 wherein the high side switch is adapted to 52. 1 be turned on for the high side on time period when the voltage across the high side 2 switch crosses below a first threshold while the high side switch is off. 3 The half bridge circuit of claim 49 wherein one of the high side on 53. 1 time period or the low side on time period is adapted to be adjusted to maintain a 2 voltage across the load during the high side on time period substantially equal to 3 the voltage across the load during the low side on time period. 4 The half bridge circuit of claim 48 wherein the voltage across the 54. 1 load is sensed for a fixed period during the high side on time period. 2 The half bridge circuit of claim 49 wherein the voltage across the 1 55.

load is sensed for a fixed period during the low side on time period.

The half bridge circuit of claim 49 wherein the delay time is 56. 1 substantially zero. 2 The half bridge circuit of claim 49 further comprising a feedback 1 57. circuit coupled between the load and the low side switch to vary the delay time to 2 regulate power delivered to the load. 3 The half bridge circuit of claim 49 wherein the low side switch is 58. 1 included in a low side integrated circuit of the half bridge circuit. 2 The half bridge circuit of claim 58 wherein the low side integrated 59. 1 circuit also comprises a low side control circuit coupled to the low side switch to 2 generate the low side on time period. 3 The half bridge circuit of claim 59 where the low side control 60. 1 circuit is coupled to sense a turn off of the high side switch 2 The half bridge circuit of claim 60 wherein the low side control 61. 1 circuit is adapted to sense the turn off of the high-side switch by monitoring the 2 voltage across the low side switch 3

l	62.	The half bridge circuit of claim 48 wherein the high side switch is
2	included in a	high side integrated circuit of the half bridge circuit.
1	63.	The half bridge circuit of claim 62 wherein the high side integrated
2	circuit also co	omprises a high side control circuit coupled to the high side switch to
3	generate the high side on time period.	
1	64.	The half bridge circuit of claim 63 wherein the high side control
2	circuit is cou	pled to sense a turn off of the low side switch.
1	65.	The half bridge circuit of claim 64 wherein the high side control
2	circuit is ada	pted to sense the turn off of the low side switch by monitoring the
3	voltage acros	ss the high-side switch.
1	66.	The half bridge circuit of claim 49 wherein the half bridge circuit is
2	included in a	switched mode power supply.
1	67.	The half bridge circuit of claim 49 wherein the half bridge circuit is
2	included in	a power conversion circuit.

the high side switch each comprise a metal oxide field effect transistor 2 3 (MOSFET). A circuit, comprising: 69. 1 switching means coupled to a load for applying a voltage of a first polarity 2 across the load during a first on time period and applying a voltage of the opposite 3 polarity during a second on time period; and 4 sensing means coupled to the load for sensing the voltage across the load 5 for a first sense period during the first on period and for a second sense period 6 during the second on period, wherein the switching means is controlled to 7 maintain a magnitude of the voltage across the load during the first on period 8 substantially equal to the voltage across the load during the second on period. 9 The circuit of claim 69 wherein the sensing means is adapted to 70. 1 generate a sense signal for a duration of the first and second sense periods. 2 The circuit of claim 70 wherein a magnitude of the sense signal is 1 71. adapted to be adjusted according to a magnitude of the voltage across the load 2 during the first and second sense periods. 3

The half bridge circuit of claim 49 wherein the low side switch and

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- 1 72. The circuit of claim 71 wherein the sensing means comprises a
- 2 capacitor and current charging means coupled to the capacitor for charging and
- 3 discharging the capacitor.
- 1 73. The circuit of claim 72 wherein the current charging means is
- 2 adapted to adjust a current for charging and discharging the capacitor in response
- 3 to the magnitude of the voltage across the load during the first and second sense
- 4 periods.